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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,384	11/26/2001	Maximilian Sergio	00AG29353319	7289

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/994,384	SERGIO ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/26/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang (US Patent # 5,847,599).

[Claim 8]

Zhang teaches a method of reading a MOS capacitive sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of MOS capacitors (imaging array 101) ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other (See figure 1), using a biasing and reading circuit comprising column and row selectors (col. 2 lines 45-47 teach control circuitry that is operative to sequential read pixels 103 will inherently have row and column selectors since they are used to selectively read pixels), and a charge amplifier (109) outputting a voltage of the pixel of a selected pixel of the array, the method comprising:

resetting an output voltage of the charge amplifier (col. 3 lines 54-61, figure 3);

connecting nonselected row and column lines of the array to a reference voltage (It would be inherent that the non selected row and column lines of the array are connected to some kind of

a reference voltage since all the pixels are shown connected to the input of the charge amplifier 105) ;

connecting one of an auxiliary capacitor (figure 2, feedback capacitor Cf) and the selected capacitor (col. 2 lines 49-54) to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor (Cf) and the selected capacitor to define a feedback capacitor of the amplifier (See figure 2);

and applying a step voltage (Vin) on the capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state (col. 3 line 62-col. 4 line 5, figure 3).

[Claim 9]

Zhang teaches wherein the reading of the sensor includes a sequential scanning of the pixels of the array, obtaining a frame of as many values of pixels of the sensor (col. 2 lines 45-65).

[Claim 10]

Zhang teaches that the scanning would be repeated with a certain frame frequency (col. 2 lines 55-65)

[Claim 11]

Zhang teaches a method of reading a capacitive MOS sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of capacitors (imaging array 101) connected in rows and columns (See figure 1), the method comprising:

providing a biasing and reading circuit comprising column and row selectors (col. 2 lines 45-47 teach control circuitry that is operative to sequential read pixels 103 will inherently have row and column selectors since they are used to selectively read pixels), an amplifier (109), connected to the column and row selectors (since the amplifier 109 is connected to array 101 through an amplifier 105, it is also connected to the control circuitry used for scanning pixels), for outputting a voltage of the capacitance of a selected capacitor of the array, and an auxiliary capacitor (Cf) connected to the column and row selectors;

connecting nonselected rows and columns of the array to a reference voltage (It would be inherent that the non selected row and column lines of the array are connected to some kind of a reference voltage since all the pixels are shown connected to the input of the charge amplifier 105) ;

connecting one of an auxiliary capacitor (figure 2, feedback capacitor Cf) and the selected capacitor (col. 2 lines 49-54) to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor (Cf) and the selected capacitor to define a feedback capacitor of the amplifier (See figure 2);

and applying a step voltage (Vin) on the capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state (col. 3 line 62-col. 4 line 5, figure 3).

[Claim 12]

Zhang teaches resetting an output voltage of the charge amplifier (col. 3 lines 54-61, figure 3);

[Claims 13 and 14]

See Examiner's notes regarding claims 9 and 10 respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US Patent # 5,847,599) in view of Smisko (US Patent # 4,902,886).

[Claim 15]

Zhang teaches a method of reading a MOS capacitive sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of MOS capacitors (imaging array 101) ordered in rows and columns, the system comprising:

a biasing and reading circuit comprising an amplifier (figure 2, element 109) for outputting a voltage representing the capacitance of a selected capacitor (col. 3 line 62-col. 4 line 5, figure 3), an auxiliary capacitor (Cf), configuration switches (S2 and S4) for coupling one of the auxiliary capacitor (Cf) and the selected capacitor (selected pixel) as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier (See figure 2).

Zhang fails to disclose an analog-to-digital converter for converting the output voltage to digital data; an input interface circuit for connecting deselected row lines and column lines of the array to a reference voltage and for coupling the selected capacitor of the capacitive sensor to the

biasing and reading circuit; a microprocessor for performing noise filtering and real-time correction of data and a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor.

However Smisko teaches an analog-to-digital converter (figure 3, A/D converter) for converting the output voltage to digital data; an input interface circuit (transfer switches 116) for connecting deselected row lines and column lines of the array to a reference voltage and for coupling the selected capacitor of the capacitive sensor to the biasing and reading circuit (transfer switch 116 connect the pixels to a resetting voltage when the resetting switch 199 is closed, col. 6 line 46-col. 7 line 46, figure 5); a microprocessor (100) for performing noise filtering (col. 6 lines 42-46) . It would be obvious to have a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor in order to use the values of the light falling on the sensor.

Therefore taking the combined teachings of Zhang and Smisko, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an analog-to-digital converter for converting the output voltage to digital data; an input interface circuit for connecting deselected row lines and column lines of the array to a reference voltage and for coupling the selected capacitor of the capacitive sensor to the biasing and reading circuit; a microprocessor for performing noise filtering and a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor in order to read out the sensor data for display and recording of the images.

Zhang in view of Smisko fail to teach real-time correction of data. However Official Notice is taken that real-time correction of data is well known in the art in order to have a

sufficiently fast and accurate system that can correct the images as fast as they are read in. Therefore taking the combined teachings of Zhang, Smisko and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have real-time correction of data is well known in the art in order to have a sufficiently fast and accurate system that can correct the images as fast as they are read in.

[Claim 16]

Smisko teaches wherein FET transfer switches (116) comprise the row and column selectors that are being controlled by the microprocessor (100) that inherently has a timing generator to read the pixels at a certain according to the timing diagram of figure 5. Smisko further teaches that the amplifier (85) and A/D converter is also controlled by the microprocessor 100 (col. 6 lines 31-52, figures 3 and 5). The timing diagram and the operation will inherently be synchronized by the microprocessor.

[Claim 17]

Smisko teaches wherein the shift register is used to read the pixels serially which means that it generates timing signals at a certain frequency (col. 1 lines 39-45). Zhang in view of Smisko fail to teach a finite state machine controlled by the microprocessor unit for configuring the shift register. However Official notice is take that it is very well known in the art to have a finite state machine that is controlled by the microprocessor unit for configuring the shift register because finite state machines can be optimized to remove redundancies and thereby reduce the time and space required to use the finite state machines. Therefore taking the combined teachings of Smisko, Zhang and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a finite state machine that is controlled by the

microprocessor unit for configuring the shift register because finite state machines can be optimized to remove redundancies and thereby reduce the time and space required to use the finite state machines.

[Claim 18]

Zhou teaches a digital shift register circuit (a selection logic circuit) controlled by the microprocessor unit 100 for producing selection signals (col. 1 lines 39-45, col. 6 lines 43-46, figures 1 and 3), and a plurality of connection modules (common node 106) for connecting the deselected rows and columns to the reference voltage (Vd), and for coupling the selected capacitor to the biasing and reading circuit based upon the selection signals (col. 1 lines 39-45).

[Claims 19-24]

These claims are a combination of claims 8, 11, 15 and 16 . Therefore these claims are rejected based upon rejected claims 8, 11, 15 and 16 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571)-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
February 27, 2007

VIVEK SRIVASTAVA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600